

XT2G201 DATASHEET

Ver-1.0

General Description

The XT2G202 is a programmable clock generator intended for high-performance consumer, networking, industrial, computing, and data-communications applications. Configurations may be stored in on-chip efuse or changed using I2C interface. The device may be configured to use one of two I2C addresses to allow multiple devices to be used in a system.

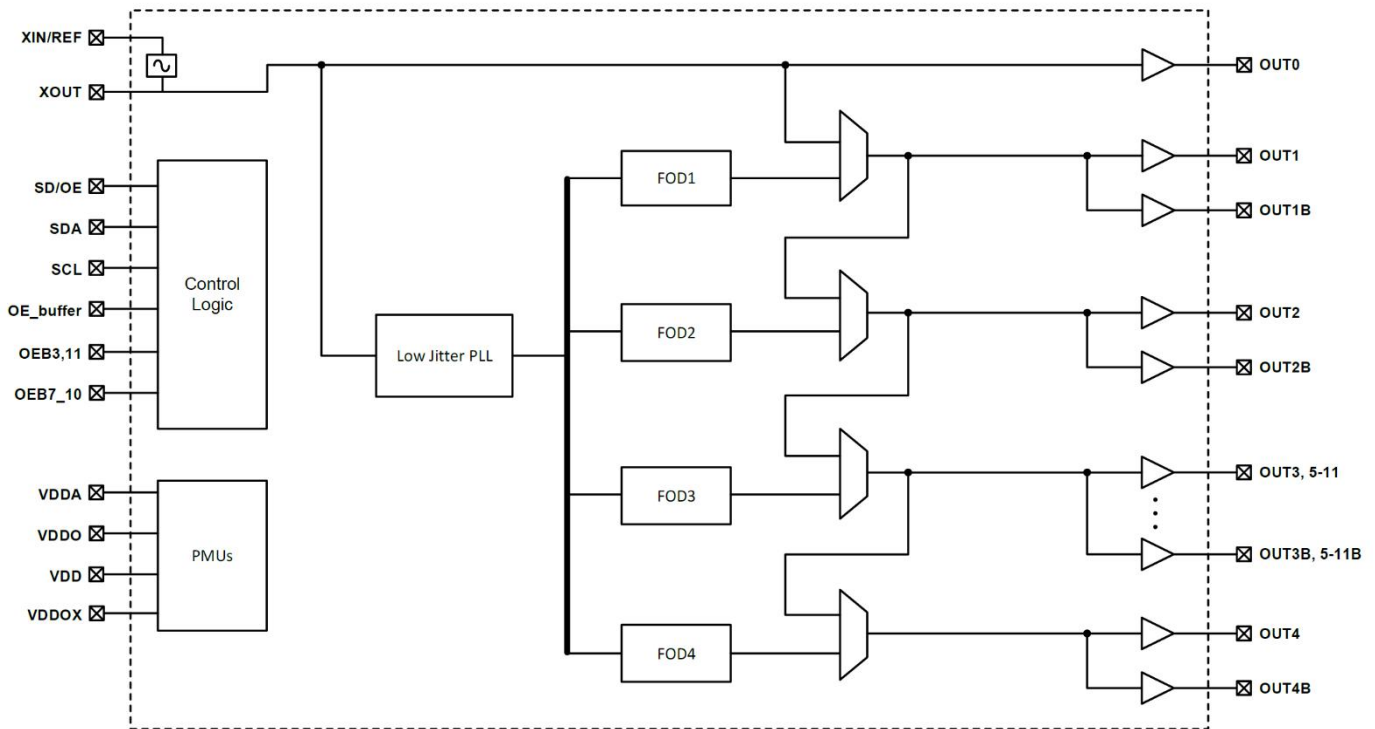
Applications

- Ethernet switch/router
- PCI Express 1.0/2.0/3.0/4.0/5.0/6.0 Spread
- Spectrum on
- Broadcast video/audio timing
- Multi-function printer
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fiber Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

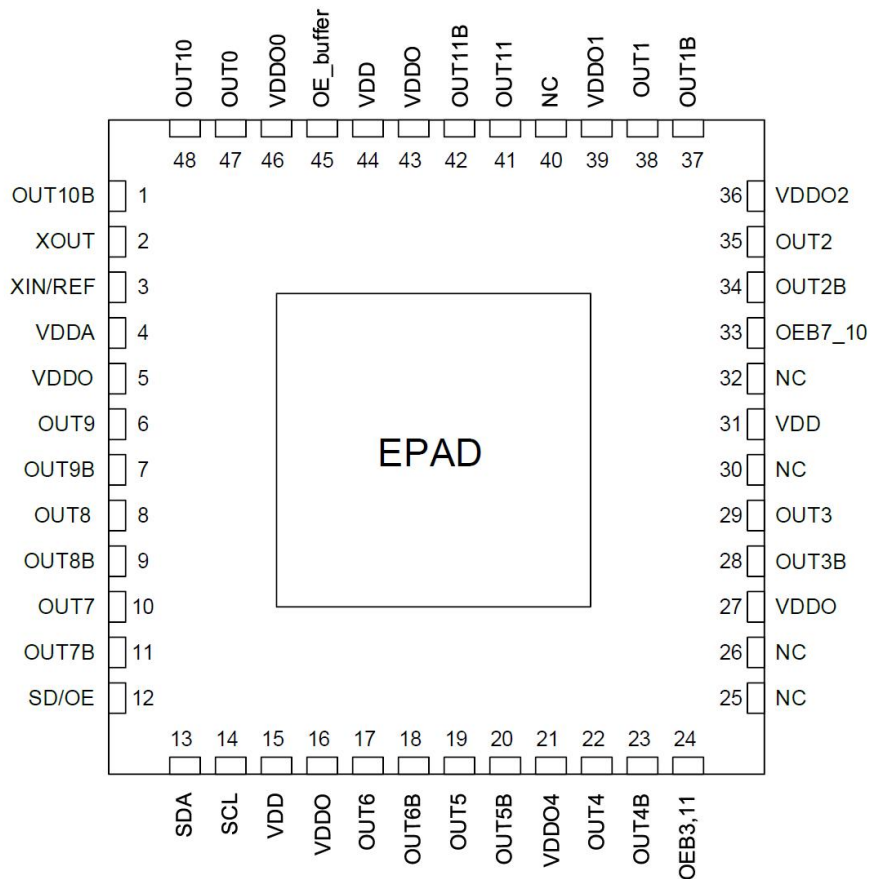
Features

- Flexible 1.8V, 2.5V, 3.3V power-rails
- High-performance, low phase noise PLL, <0.5ps RMS typical phase jitter on outputs
- Generates up to four independent output frequencies with a total of 11 differential outputs and one reference output
- Supports multiple differential output I/O standards:
 - Three universal outputs pairs with each configurable as one differential output pair (LVDS, LVPECL or regular HCSL) or two LVCMOS outputs. Frequency of each output pair can be individually programmed
 - Eight copies of Low Power HCSL(LP-HCSL) outputs. Programmable frequency.
- One reference LVCMOS output clock
- Four fractional output dividers (FODs)
- Input frequency ranges:
 - Crystal frequency range: 8MHz to 100MHz
- Output frequency ranges:
 - LVCMOS Clock Outputs – 1MHz to 200MHz
 - LP-HCSL Clock Outputs – 1MHz to 200MHz
 - Other Differential Clock Outputs – 1MHz to 300MHz
- Programmable crystal load capacitance
- Power-down mode
- I2C serial programming interface
- Available in 6 × 6 mm 48-pin QFN package
- -40° to +85°C industrial temperature operation applications

Block Diagram:



Pin Configuration:



48-pin QFN

Pin Descriptions:

Number	Name	Type	Description
1	OUT10B	Output	Complementary output clock 10. Low-Power HCSL (LP-HCSL) output.
2	XOUT	Input	Crystal oscillator interface output.
3	XIN/REF	Input	Crystal oscillator interface input, or single-ended LVCMOS clock input. Ensure that the input voltage is 1.8V max.
4	VDDA	Power	Analog functions power supply pin. Connect to 1.8V to 3.3V. VDDA and VDD should have the same voltage applied.
5	VDDO	Power	Connect to 1.8V. Power pin for outputs 3, 5-11.
6	OUT9	Output	Output clock 9. Low-Power HCSL (LP-HCSL) output.
7	OUT9B	Output	Complementary output clock 9. Low-Power HCSL (LP-HCSL) output.
8	OUT8	Output	Output clock 8. Low-Power HCSL (LP-HCSL) output.
9	OUT8B	Output	Complementary output clock 8. Low-Power HCSL (LP-HCSL) output.
10	OUT7	Output	Output clock 7. Low-Power HCSL (LP-HCSL) output.
11	OUT7B	Output	Complementary output clock 7. Low-Power HCSL (LP-HCSL) output.
12	SD/OE	Input	Enables/disables the outputs (OE) or powers down the chip (SD). Weak internal pulldown resistor.
13	SDA	Input	I2C SDA input.
14	SCL	Input	I2C SCL input.
15	VDD	Power	Connect to 1.8V to 3.3V.
16	VDDO	Power	Connect to 1.8V. Power pin for outputs 3, 5-11.
17	OUT6	Output	Output Clock 6. Low-Power HCSL (LP-HCSL) output.
18	OUT6B	Output	Complementary Output Clock 6. Low-Power HCSL (LP-HCSL) output.
19	OUT5	Output	Output Clock 5. Low-Power HCSL (LP-HCSL) output.
20	OUT5B	Output	Complementary output clock 5. Low-Power HCSL (LP-HCSL) output.
21	VDDO4	Power	Connect to 1.8V to 3.3V. VDD supply for OUT4.
22	OUT4	Output	Output clock 4.
23	OUT4B	Output	Complementary output clock 4.
24	OEB3,11	Input	Active low Output Enable pin for Outputs 3, 5, 6, 11. 1 = disable outputs, 0 = enable outputs. This pin has internal pull-down.
25	NC	Input	Do not connect.
26	NC	Input	Do not connect.
27	VDDO	Power	Connect to 1.8V. Power pin for outputs 3, 5-11.
28	OUT3B	Output	Complementary output Clock 3. Low-Power HCSL (LP-HCSL) output.
29	OUT3	Output	Output clock 3. Low-Power HCSL (LP-HCSL) output.
30	NC	Input	Do not connect.
31	VDD	Power	Connect to 1.8V to 3.3V.
32	NC	Input	Do not connect.
33	OEB7_10	Input	Active low Output Enable pin for Outputs 7-10. 1 = disable outputs, 0 = enable outputs. This pin has internal pull-down.
34	OUT2B	Output	Complementary output clock 2.
35	OUT2	Output	Output clock 2.
36	VDDO2	Power	Connect to 1.8V to 3.3V. VDD supply for OUT2.
37	OUT1B	Output	Complementary output clock 1.
38	OUT1	Output	Output clock 1.
39	VDDO1	Power	Connect to 1.8V to 3.3V. VDD supply for OUT1.
40	NC	Input	Do not connect.



41	OUT11	Output	Output clock 11. Low-Power HCSSL(LP-HCSSL) output.
42	OUT11B	Output	Complementary output clock 11. Low-Power HCSSL(LP-HCSSL) output.
43	VDDO	Power	Connect to 1.8V. Power pin for outputs 3, 5-11
44	VDD	Power	Connect to 1.8V to 3.3V. VDDA and VDD should have the same voltage applied.
45	OE_buffer	Input	Active High Output enable for outputs 3, 5-11. 0 = disable outputs, 1=enable outputs. This pin has internal pull-up.
46	VDDO0	Power	Power supply pin for OUT0. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
47	OUT0	Output	Output clock 0, the pin acts as a LVCMOS reference output.
48	OUT10	Output	Output clock 10. Low-Power HCSSL (LP-HCSSL) output.
EPAD	GND	GND	Connect to ground pad